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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/058,681	01/28/2002	Ming-Nan Yen	JCLA7301	4020

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EXAMINER	
GHEBRETINSAE, TEMESGHEN	
ART UNIT	**PAPER NUMBER**
2637	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/058,681	YEN ET AL.	
	Examiner	Art Unit	
	Temesghen Ghebretinsae	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6,8,9 and 11-14* is/are rejected.

7)☐ Claim(s) *3,7,10 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It would be of great assistance to the Office if all incoming papers pertaining to a filed application carried the following items:

1. Application number (checked for accuracy, including series code and serial no.).
2. Group art unit number (copied from most recent Office communication).
3. Filing date.
4. Name of the examiner who prepared the most recent Office action.
5. Title of invention.
6. Confirmation number (See MPEP § 503).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1,5,6,9,11and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bray et al. (5,373,255) in view of Lee et al (6,392,496)

4. Bray discloses a digital phase locked loop (fig.2) comprising: means (41,42) for comparing a feedback signal and a reference signal; sampling (sampling clock) the compared result at a predetermined frequency; means (44) for outputting signal at the output frequency; and means (45) for feeding back (a feedback signal with a feedback frequency) and dividing down the output from the VCO. An up-down converter (41) as claimed in claim 6. The post adjusting value for the post divider is adjustable (N) as claimed in claim 9. The feedback signal has a preset value as claimed in claim 11. The

post adjusting value is set according to the required output frequency as claimed in claim 13. (See col.3, line to col. 4, line 47).

Bray differs from the claimed invention in that he does not have DAC for converting the digital phase adjusting signal into an analog phase adjusting signal. However, Lee discloses a PLL having a DAC for converting the digital phase adjusting signal into an analog phase adjusting signal. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to add a DAC in the circuit of Bray to convert the digital phase adjusting signal of Bray into an analog phase adjusting signal since DAC are well know in converting digital signal into analog signal. Furthermore it is obvious in communication art to convert the digital phase adjusting signal into analog if the VCO is analog circuit.

5. Claims 1,5,6,9,11and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bray et al. (5,373,255) in view of Wereker et al (5,856,762).

6. Bray discloses a digital phase locked loop (fig.2) comprising: means (41,42) for comparing a feedback signal and a reference signal; sampling (sampling clock) the compared result at a predetermined frequency; means (44) for outputting signal at the output frequency; and means (45) for feeding back (a feedback signal with a feedback frequency) and dividing down the output from the VCO. An up-down converter (41) as claimed in claim 6. The post adjusting value for the post divider is adjustable (N) as claimed in claim 9. The feedback signal has a preset value as claimed in claim 11. The

post adjusting value is set according to the required output frequency as claimed in claim 13. (See col.3, line to col. 4, line 47).

Bray differs from the claimed invention in that he does not have DAC for converting the digital phase adjusting signal into an analog phase adjusting signal. However, Wereker discloses a digital phase locked loop comprising: a phase detector for comparing a feedback signal and a reference signal (51); a digital to analog converter for converting the digital phase to analog phase signal (53); a voltage control oscillator (4) and a post divider (13) for feeding back (a feedback signal with a feedback frequency) and dividing down the output from the VCO (13) (See fig.1 and col.3, line 40 to col.4, line 6). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to add a DAC in the circuit of Bray to convert the digital phase adjusting signal of Bray into an analog phase adjusting signal since DAC are well know in converting digital signal into analog signal. Furthermore it is obvious to convert the digital phase adjusting signal into analog if the VCO is analog circuit.

7. Claims 2,4,8,12,14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bray in view of Lee further in view of Berry et al (6,366,174).

Bray and Lee discloses the claimed subject matter as described above. Bray and Lee differ from the present claimed invention in that Both are silent about pre-divider as claimed in claim 2 and 12; out put divider as claimed in claim 4 and 14; However, Berry discloses a phase locked loop apparatus comprising: an adjustable pre-divider for dividing down the input signal (20); and adjustable output divider (44). Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made

to modify Bray's PLL circuit to show the pre-divider and output divider. One would be motivated to do so because having a PLL circuit with optional frequency multiply or frequency divide circuits can improve the latch time. (See Berry col.2, lines 1-15. and fig.1) As for the built-in self-tester, such is well know in the art (see specification page 8, lines 21-22.)

8. Claims 2,4,12,14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bray in view of Werker further in view of Berry

Bray and Werker disclose the subject matters claimed in claims 1,5,6,9,11,13 as described above. Bray and Werker differs from the present invention in that Both are silent about pre-divider as claimed in claim 2 and 12; out put divider as claimed in claim 4 and 14. However, such are disclosed by Berry and are well know in the PLL circuit and would have been obvious to have a PLL circuit with optional frequency multiply or frequency divide circuits so that the latch (lock) time can be improved. (See Berry col. 2, lines 1-15 and fig.1).

Allowable Subject Matter

9. Claim 3,7,10,15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

10. Applicant's arguments filed 12/1/05 have been fully considered but they are not persuasive. . Applicant argues that the prior art does not disclose "means for comparing a feedback signal with a feedback frequency and reference signal at a frequency,

sampling the compared result at predetermined frequency, and outputting a digital phase adjusting signal" as claimed in claim 1. Furthermore applicant argues, "the scope pf the phase digital converter as claimed in claims 1" can not be pieced to be identical to the combination of phase detector 41 and phase accumulator 42 a s disclosed in Bray.

But examiner disagree with applicant because Bray does disclose "a means for comparing a feedback signal with a feedback frequency and reference signal at a frequency, sampling the compared result at a predetermined frequency" see fig.2 (41-41). Thus phase detector 41 and phase accumulator 42 do function same as the phase detector of the present claimed invention. That is comparing a feedback signal and a reference signal; sampling (sampling clock) the compared result at a predetermined frequency.

See making a prima facie case of equivalence 54 USPQ2d 1308(Fed Cir. 2000) and MPEP 2183 A.

2183 Making a Prima Facie Case of Equivalence

If the examiner finds that a prior art element

(A) Performs the function specified in the claim,

(B) is not excluded by any explicit definition provided in the specification for an equivalent, and

(C) is an equivalent of the means- (or step-) plus-function limitation,

the examiner should provide an explanation and rationale in the Office action as to why the prior art element is an equivalent. Factors that will support a conclusion that the prior art element is an equivalent are:

(A) The prior art element performs the identical function specified in the claim in substantially the same way, and produces substantially the same results as the corresponding element disclosed in the specification. Kemco Sales, Inc. v. Control

Papers Co., 208 F.3d 1352, 54 USPQ2d 1308 (Fed. Cir. 2000)

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Temesghen Ghebretinsae whose telephone number is 571-272-3017. The examiner can normally be reached on Monday-Friday from 8 to 5. The examiner can also be reached on alternate

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel, can be reached on 572-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Temesghen Ghebretinsae
Primary Examiner
Art Unit 2637

T.G.

2/15/06.

TEMESGHEN GHEBRETINSAE
PRIMARY EXAMINER